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Note : Remove “Table of Content” before including in CP Book

18ECL37 : ANALOG ELECTRONICS LABORATORY

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	BE	*Program:*	EC
Year / Semester :	2 / 3	*Academic Year:*	2019-20
Course Title:	ANALOG ELECTRONICS LAB	*Course Code:*	18ECL37
Credit / L-T-P:	3/ 3-0-0	*SEE Duration:*	
Total Contact Hours:	Hrs	*SEE Marks:*	
CIA Marks:	40	*Assignment*	1 / Module
Course Plan Author:	Mrs. Amaresh C	*Sign*	Dt :
Checked By:		*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier (b) Bridge Rectifier	3	Rectifier Characteristics	L4 Analyze
2	Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).	3	Diode Clipping & Clamping	L4
3	Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.	3	Regulator Characteristics	L4
4	Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.	3	BJT Emitter follower gain& impedances	L4
5	Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain-bandwidth product from its frequency response.	3	BJT common emitter gain & frequen	L4

			cy	
6	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.	3	transfer and drain characteristics of JFET	L4
7	Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.	3	Frequency response of JFET/MOSFET	L4
8	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.	3	characteristics of n-channel MOSFET	L3
9	Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.	3	push pull power amplifier efficiency	L4
10	Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.	3	Study of RC phase shift oscillator waveforms	L4
11	Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a) Hartley Oscillator (b) Colpitts Oscillator	3	Frequency of oscillation of hartley& colpitts Oscillator	L4
12	Design and set-up the crystal oscillator and determine the	3	Frequen	L4

	frequency of oscillation.		cy of oscillation of crystal oscillator	

3. Lab Material

Unit	Details	Available
1	Text books	
	1. Robert L. Boylestad and Louis Nashelsky, "Electronics devices and Circuit theory",Pearson, 10th Edition, 2012, ISBN: 978-81-317-6459-6.	In Lib
2	Reference books	
	1. Adel S. Sedra and Kenneth C. Smith, "Micro Electronic Circuits Theory And Applicatication," 5th Edition ISBN:0198062257	In dept
	2. Fundamentals of Microelectronics, Behzad Razavi, John Weily ISBN 2013 978-81-265-2307-8	
	3. J.Millman & C.C.Halkias—Integrated Electronics, 2 nd edition, 2010, TMH. ISBN 0-07-462245-5	
	4. K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5th Edition, 2015, ISBN:9788120351424.	
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	18ELN14	Basic Electronics	Knowledge on basic componentslike diode, rectifiers, transistors etc	1	
				-	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

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5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the Experiment, certification/Sign of the concerned staff in-charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings/observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified/Signed by staff member in-charge.	
6	Should attempt all Experiments / assignments given in the list of contents in Lab manual,session wise.	
7	When the experiment is completed, should disconnect the setup made by them, and should return all the components/instruments taken for the purpose of experiment conduction.	
8	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
9	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the Circuit diagram, do the necessary calculations with the values given for the circuit components and output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Start writing the circuit diagram	
2	Do the required calculations and find the values of components	
3	Replace the components with the calculated values in the circuit diagram	
4	Make the connections as per circuit diagram	
5	Turn on the power supply and CRO	
6	Check for the output as per the calculations	
7	Check for the Errors in connection and correct it	
8	Write down the reading and output value and compare	
9	Perform the Experiment	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	Understand and design wave shaping circuits	03	Clipping and clamping	Demonstrate	Test	L4
2	Apply mathematics and concepts of fundamentals to design electronics circuits	03	Amplifiers	Demonstrate	Test	L4
3	Conduct an experiment to verify the device characteristics	03	Rectification Regulation	Demonstrate	Test	L4
4	Design a simple electronic circuit for a given specifications	03	Oscillators	Simulation	Test	L4
5	To estimate the parameters through experiments and analyse the performance of the given circuits	03		Demonstrate	Test	L4
-	**Total**	**15**	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	To determine the amplitude of the modulating signals & used to supply steady and polarized Dc voltage in the electric welding.	CO1	L4
2	Used in speech processing for communications (radio) applications & audio compression.	CO2	L4
3	Used in RF,radio, small power supply units, medical field etc	CO3	L3
4	In some Capacitor to power the high-side NMOS driver.	CO4	L3
5	Apply voltage divider bias to find gain bandwidth & frequency response	CO5	L3
6	Used in buffer amplifier,electronic switch, phase shift oscillator etc	CO6	L3
7	widely used for switching and amplifying electronic signals in the electronic devices.	CO7	L3
8	Switching circuits	CO8	L3
9	used in low-cost design devices and mobile devices	CO9	L4
10	musical instruments, voice synthesis and in GPS units since they work at all audio frequencies.	CO10	L4
11	Used in radio receivers, oscillations in RF, sensors, mobile and radio communications.	CO11	L4

12	frequency-determining component, a wafer of quartz crystal or ceramic with electrodes connected to it.	CO12	L4

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	Level
1	Understand and design wave shaping circuits	3	3	1	2	2	–	–	–	--	–	–	–	L4
2	Apply mathematics and concepts of fundamentals to design electronics circuits	3	3	1	2	2	–	–	–	–	–	–	–	L4
3	Conduct an experiment to verify the device characteristics	3	3	1	2	2	–	–	–	–	–	–	–	L4
4	Design a simple electronic circuit for a given specifications	3	3	1	2	2	–	–	–	–	–	–	–	L4
5	To estimate the parameters through experiments and analyse the performance of the given circuits	3	3	1	2	2	–	–	–	–	–	–	–	L4

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Mapping Level	Justification
CO	**PO**	**-**	**-**
CO1	PO1	L4	Wave shaping circuits require the basic knowledge of components , value calculation and designing of circuits using them.
CO1	PO2	L4	Analysis of different voltage clipping levels as problem analysis is done
CO1	PO3	L4	Different levels and patterns of clipping is done which gives us various design solutions
CO1	PO4	L4	Basic knowledge of designing is required to help circuits to be used in different higher end circuits.
CO1	PO5	L4	Modern tools can be used to realize the circuits in software and vary to get different levels of voltage.

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CO2	PO1	L4	Knowledge of engineering fundamentals is required to design amplifier circuits with specific gain.
CO2	PO2	L4	Analyze the gain needed and design accordingly the parameters in the circuit
CO2	PO3	L4	Basic level of solution development is done using amplifier circuits.
CO2	PO4	L4	Investigations regarding gains is done by plotting graph and calculating bandwidth for the amplifier
CO2	PO5	L4	Modern tools can be used to realize the circuits in software and also cascading of circuits can be done to increase the gain.
CO3	PO1		Knowledge of engineering fundamentals is required to design Rectification circuits with different regulation levels
CO3	PO2	L4	Regulation of different voltage levels can be done and ripple factor , deficiency calculations is done to analyze the circuits.
CO3	PO3	L4	Basic level of solution development is done using Rectification circuits.
CO3	PO4	L4	Investigations regarding efficiency is done for different rectification circuits.
CO3	PO5	L4	Modern tools can be used to realize the circuits in software making analysis easier.
CO4	PO1	L4	Knowledge of engineering fundamentals is required to design oscillator circuits with specific gain.
CO4	PO2	L4	Analyze the circuits design accordingly the parameters in the circuit for given frequency.
CO4	PO3	L4	Basic level of solution development is done using oscillator circuits.
CO4	PO4	L4	Investigations regarding tank circuit is done for generating sustained oscillations
CO4	PO5	L4	Modern tools can be used to realize the circuits

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

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6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1		03									
2		03									
3		03									
4		03									
5		03									
6		03									
7		03									
8		03									
9		03									
10		03									
11		03									
12		03									
-	**Total**	**36**	**12**						**12**	-	-

Note: Write CO based on the theory course.

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2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1			
CIA Exam – 2			
CIA Exam – 3			
Assignment – 1			
Assignment – 2			
Assignment – 3			
Seminar – 1			
Seminar – 2			
Seminar – 3			
Other Activities – define – Slip test		CO1 to Co9	L2, L3, L4 . ..
Final CIA Marks	**40**	**-**	**-**

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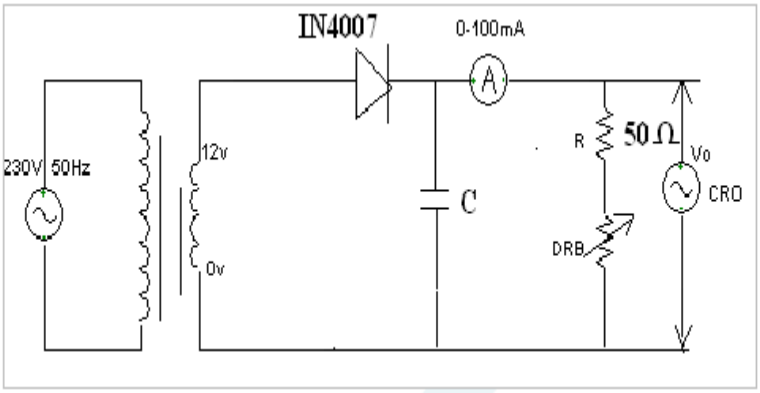
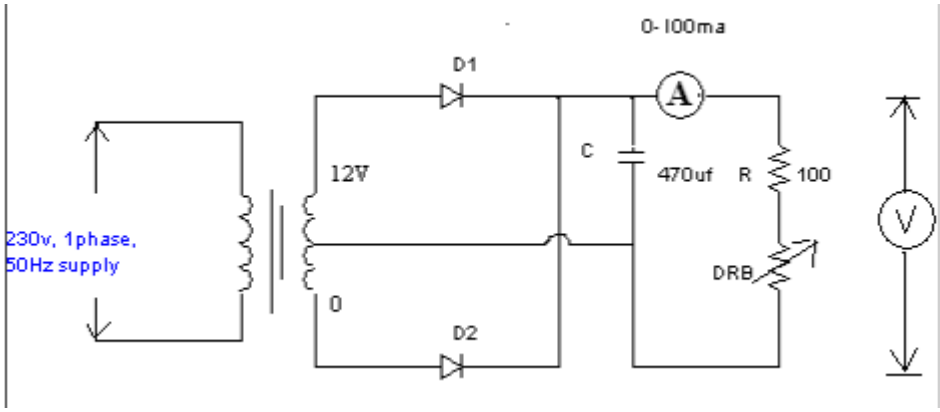
SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	25 Marks
4	Internal Assessment	40 Marks
5	SEE	60 Marks
-	**Total**	**100 Marks**

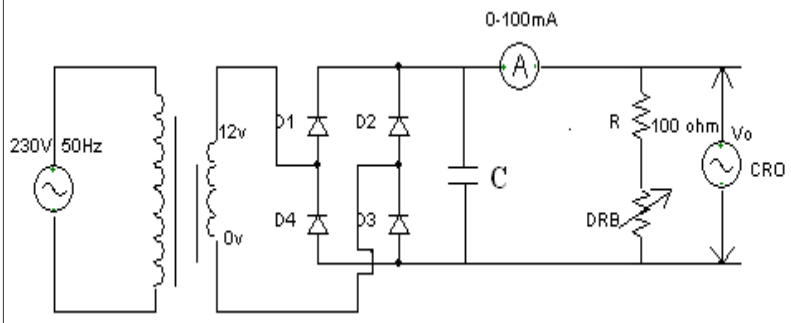
D. EXPERIMENTS

Experiment 01 : RECTIFIER CIRCUITS

–	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier (b) Bridge Rectifier						
2	Course Outcomes	Design Full wave & Bridge rectifier and determine ripple factor & efficiency.						
3	Aim	Testing of Half wave , Full wave and Bridge Rectifier circuits with and without capacitor filter. Determination of ripple factor, regulation and						

		efficiency.
4	Material/ Equipment Required	Lab Manual Switching diode – Step-down transformer with center tap secondary (230/12V-0-12V), diode 1N4007, Resistor 100ohm, Capacitor 470uf Resistors 50 ohm and DRB, bread board, Wires CRO & multimeter for testing
5	Theory, Formula, Principle, Concept	**Theory:** – A rectifier converts ac to dc . Rectifiers are used in the design of dc power supplies required for all electrical circuits to work. A semiconductor diode conducts only in one direction. This property is used in the design of rectifier circuit. Based on the output there are mainly two types of rectifiers namely half wave and full wave rectifiers. As the Dc output voltage is in pulsed form, capacitor is used to filter it. The main purpose of conducting this test is to understand the application of diode in half wave and full wave rectifier circuits and to understand how to get ripple free output using capacitor filter. Half wave single phase rectifiers: – The Half wave rectifier is a circuit, which converts an ac voltage to dc voltage. In the Half wave rectifier circuit shown, the transformer serves two purposes. 1.It can be used to obtain the desired level of dc voltage (using step up or step down transformers). 2.It provides isolation from the power line. Full wave single phase rectifier:–Both cycles are rectified and ripple factor will be less and efficiency increases.. Based on the construction, there are mainly two types of full wave rectifiers a) Center tap full wave rectifier:– In this configuration, only 2 diodes are sufficient, but transformer with center tap secondary is must. Peak inverse voltage of the diode is twice the input voltage. b) Full wave bridge rectifier:– 4 diodes are required and can be applied without transformer also. As two diodes are in series with each cycle, the voltage drop across the diode is twice that of in the center tap transformer. So at very low voltage this is not suitable.
6	Procedure	• Draw the circuit, expected waveform, design the transformer ratio in the circuit • Place the components on bread board and connect them as per fig 1. Use the wires for connection as required. • Set the DRB to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter. Also note down readings of V_{ac}, V_{dc} with the same multimeter. Value of V_{dc} for DRB set to maximum is designated as no-load voltage $V_{dc(NL)}$.Tabulate the readings and find out ripple factor, load regulation, and efficiency.

		• Using CRO measure the out put wave form and sees that it matches with required wave form. Note down input & output wave form and draw it on graph. • Repeat this experiment for half wave rectifier by connecting the suitable capacitor across the load to reduce the ripple to less than 8% • Repeat this experiment for both type full wave rectifiers without and with capacitorfficiency • step 7:Disconnect the circuit
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• **A) Half Wave Rectifier without & with filter** **Circuit Diagram:**  **B) Full wave Rectifiers** **Circuit Diagram:** **Full wave rectifier with C filter (Remove C for rectifier without filter)**  **Full wave bridge rectifier with C filter (Remove C for rectifier without filter)**



8 Observation Table, Look-up Table, Output

A) Half Wave Rectifier without & with filter

Readings

Vin (ac)= ---------- V_{NL} = --------- (With load removed or keeping load resistance >100K)

R_L	Iac(mA)	Idc(mA)	Vo(dc)	Vo(ac)	Ripple = Vo(ac)/Vo(dc)	Efficiency	Regulation

With C Filter

Idc	Vm	Vr_(p-p)	Vdc=Vm – (Vr_p-p/2)	Vr_rms = Vr(p-p)/(2√3)	γ = Vr_rms/Vdc

B) Full wave Rectifiers

Readings

Vin (ac)= ---------- V_{NL} = ----------(With load removed or keeping load resistance >100K

RL	Iac(mA)	Idc(mA)	Vo(dc)	Vo(ac)	Ripple = Vo(ac)/Vo(dc)	Efficiency	Regulation

with C filter

Idc	Vm	Vr_(p-p)	Vdc=Vm – (Vr_p-p/2)	Vr_rms = Vr(p-p)/(2√3)	γ = Vr_rms/Vdc

9	Sample Calculations	**A) Half Wave Rectifier without & with filter** **Design: Without Filter** Vin(ac) = rms value of input(secondary of the transformer), Vo(dc) = Average value of dc output

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Vo(ac) = rms value of ac component of the output voltage

Let Vo(dc) = 5V , Idc =100mA for HWR output wave, Vdc= Vm/ π

Vm = Vo(dc) x **ΤΤ** = 15.7V for Sinusoidal input wave, Vrms= Vm/$\sqrt{2}$

Vin(ac rms) = Vm/$\sqrt{2}$ =11.13V ➔ 12V (Connect two end terminals of transformer secondary)

So Rload =5V/100mA =50 ohm

With Filter

Vdc=Vm-Vr(p-p)/2

Let Ripple factor, r < 0.08 or 8%, Vo(dc) = 10V ,

I_{dc} =100mA

r = 1 / (2 x$\sqrt{3}$ fCR_L)

f=50Hz, r=0.08 $R_{L=}$ 100Ω., substitute and calculate C value.

C= 470uF

Wkt $Vrms = Vm/2$

$Vdc = Vm/\prod$

Calculations:

Ripple factor, r = rms value of ac component / Value of dc component = Vo(ac)/Vo(dc) **or** Iac/Idc

% Efficiency η = output power /Input power =Idc^2 * 100 /(Iac^{2+} Idc^2))

% Regulation = [(V_{NL} -V_{FL})/V_{FL}]*100

B) Full wave Rectifiers

Design: Without Filter

Let Vo(dc) = 10V, Idc =100mA. for FWR output wave, Vdc= 2Vm/ π

Vm = Vo(dc) x π/2 = 15.7V

Vin(rms) = Vm/$\sqrt{2}$ = 11.1V (Use 12V transformer)

Vdc=Idc x R_L

So R_L =Vdc/Idc = 10V/100mA =100 ohm

With Filter

Vdc=Vm-Vr(p-p)/2

Let Ripple factor, r = 0.04 or 4%, Vo(dc) = 15V , Idc =100mA

r = 1 / (4 x$\sqrt{3}$ fCR_L)

Take C= 470uF

Wkt $Vrms = Vm/\sqrt{2}$
$Vdc = 2Vm/\prod$

Calculations:

Ripple factor, r = rms value of ac component / Value of dc component

= Vo(ac)/Vo(dc) **or** Iac/Idc

% Efficiency η = output power /Input power =Idc^2 * 100 /(Iac^{2+} Idc^2))

% Regulation = [(V_{FL} –V_{FL})/V_{FL}]*100

10	Graphs, Outputs	**A) Half Wave Rectifier without & with filter**

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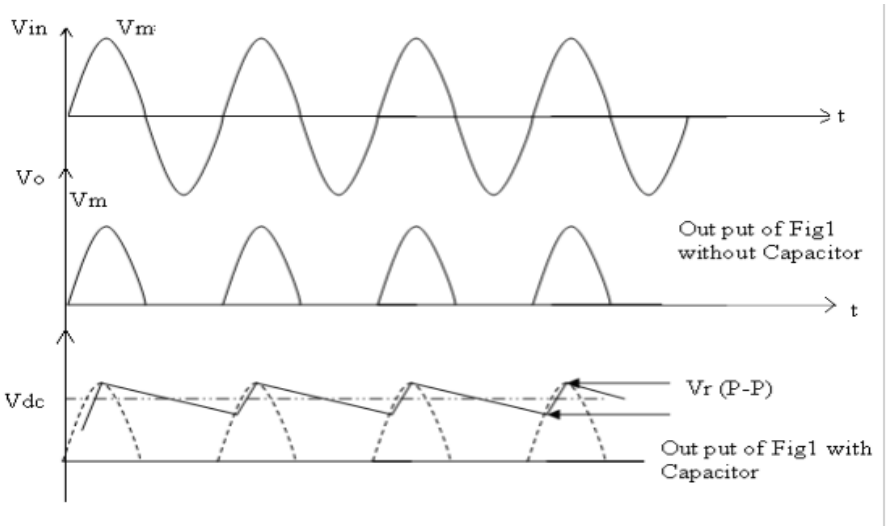
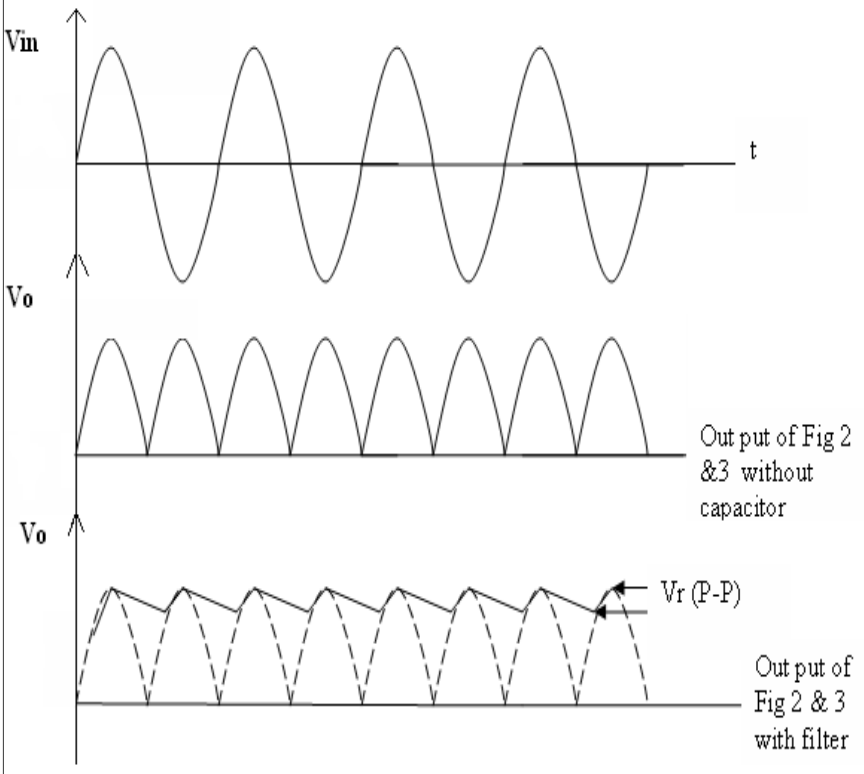
Waveforms:



B) Full wave Rectifiers



11	Results & Analysis	**Result :-** The performance of all the three rectifiers are checked
12	Application Areas	• To determine the amplitude of the modulating signals & used to supply steady and polarized Dc voltage in the electric welding.
13	Remarks	
14	Faculty Signature with Date	

Circuit	Ripple factor γ	Efficiency η	Regulation
HWR without filter			
HWR with C filter			
FWR -center tap without filter			
FWR -center tap with C filter			
FWR -Bridge without filter			
FWR -Bridge with C filter			

Experiment 02 : Clipping & clamping

–	**Experiment No.:**	2	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).						
2	Course Outcomes	Understanding Clipping and Clamping						
3	Aim							
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	To identify the clipping & clamping waveforms in the CRO To do the calculations						
6	Procedure, Program, Activity, Algorithm, Pseudo	Step 1: start by Designing the circuit using bread board Step 2: See the wave forms for clipping & clamping (positive & negative) Step 3: Write the same in observation						

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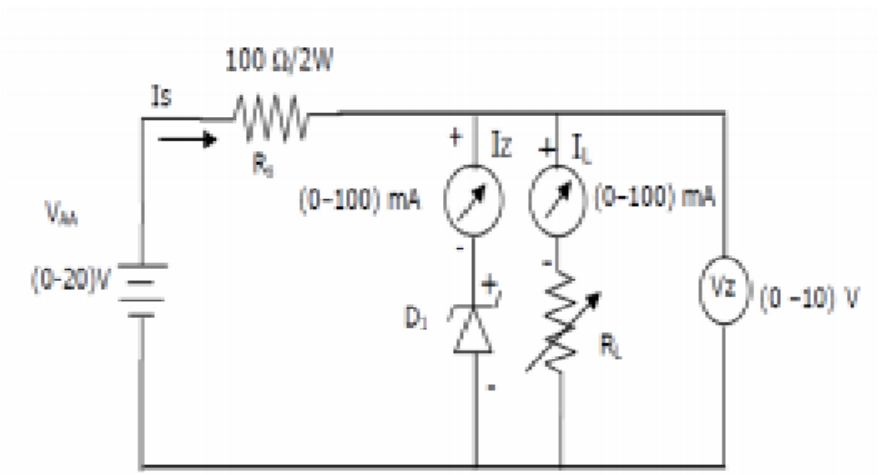
	Code	Step 4: do the calculations Step 5: Disconnect the circuit
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	Write down the wave forms of clipping & clamping for different values
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	Used in speech processing for communications (radio) applications & audio compression.
13	Remarks	
14	Faculty Signature with Date	

Experiment 03 : **Zener Diode as Voltage Regulator**

-	**Experiment No.:**	3	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.						
2	Course Outcomes	Determine the Voltage regulator line & load characteristics.						
3	Aim	To study zener diode as voltage regulator and calculate % of load regulation.						
4	Material / Equipment Required	Lab Manual Zener diode(), Resistance (100Ω/2W , Load Resistance), Power Suply(0-30V), Multimeter Circuit Diagram						
5	Theory, Formula, Principle, Concept	**Theory:** Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. It is acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode break downs while reverse biased. In the case of normal diodes the diode damages at the break down voltage. But Zener diode is specially designed to operate in the reverse breakdown region. The basic principle of Zener diode is the Zener breakdown. When a diode is						

		heavily doped, it's depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction. And the electron hole pair generation takes place. Thus heavy current flows. This is known as Zener break down. So a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage across it remains constant. This principle is used in voltage regulator using Zener diodes. The figure shows the zener voltage regulator, it consists of a current limiting resistor RS connected in series with the input voltage Vs and zener diode is connected in parallel with the load RL in reverse biased condition. The output voltage is always selected with a breakdown voltage Vz of the diode.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	A) Load Regulation: 1. For finding load regulation, make connections as shown in figure below. 2. Keep input voltage constant say 10V, vary load resistance value. 3. Note down no load voltage 'VNL' for maximum load resistance value and full load voltage 'VFL' for minimum load resistance value. 4. Calculate load regulation using, % load regulation = (VNL-VFL)/ VFL x100
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 Load Regulation: Zener Regulator

8	Observation Table, Look-up Table, Output	Write down the characteristics graph
9	Sample Calculations	
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	Used in RF,radio, small power supply units, medical field etc
13	Remarks	
14	Faculty Signature with Date	

Experiment 04 : EMITTER FOLLOWER Using Voltage Divider BIAS

-	**Experiment No.:**	4	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.						
2	Course Outcomes	Realize BJT darlington emitter follower gain, input & output impedances						
3	Aim	Design of a BJT Darlington emitter follower and determine the gain, input and output impedances.						
4	Material / Equipment Required	Lab Manual Bread board, NPN transistors (SL100), Resistors, Capacitors, VRPS (0-30Vdc), Signal generator, CRO for testing						
5	Theory, Formula, Principle, Concept	**Theory:** The emitter follower has reasonably high input impedance and may be used wherever input impedance up to about 500 K Ohms is needed. For higher input impedance, we may use 2 transistors to form what is called a Darlington pair. When the output is taken from the Emitter terminal of the transistor, the network is referred to as an Emitter follower. The output voltage is always less than the input voltage due to the drop between the base and emitter. However, the voltage gain is usually approximated to one. In addition, the output is having the same polarity as the input voltage. Hence it is said to follow the input voltage with an in-phase relationship. This accounts for the terminology 'Emitter – follower'. For ac analysis, the						

		collector is grounded, therefore the circuit is actually a common-collector configuration. This circuit presents high impedance at the input and low impedance at the output. It is therefore frequently used for impedance matching purposes, where a load is matched to the source impedance for maximum signal transfer through the system. The Darlington connection shown is a connection of two transistors whose result is a current gain that is the product of the current gains of the individual transistors. Hence the Darlington pair operates as one 'Super beta' transistor offering a very high current gain. Thus the Darlington Emitter follower is a CC configuration that has the following characteristics: Voltage gain → almost unity Current gain → very high, a few thousands Input impedance → high, hundreds of Kilo ohms Output impedance → low, tens of ohms **Darlington Emitter follower with Bootstrap** The biasing network reduces the input impedance of the amplifier. This is because of the considerable amount of current it takes. By h-parameter model input impedance is the parallel combination of input resistance of the transistor and of the biasing network. The biasing network resistance is always less than the resistance of the transistor. To improve the resistance of the circuit, a series circuit consisting of a resistor and a capacitor is connected between the emitter and the base. This process of connecting output to input through a resistor under ac conditions is called Bootstrapping
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Darlington emitter follower without bootstrap** **Procedure:** 1. To find Q-point: Connect the circuit without Ac supply .Set Vcc=10V. Measure the DC voltage (using CRO/multimeter) at the (V_{B2}), Collector (V_{C2}) emitter (V_{E2}) w.r.t ground. Then determine $VC_{E2}= V_{C2} – VE_2$, $I_{C2}=I_{E2}=V_{E2} / R_E$ 2. Q point = (Vce_2, Ic_2) 3. Connect the signal generator and apply a sine wave of peak-to-peak amplitude 1V, 1kHz from the signal generator and note down the output wave form. 4. Gradually increase the input signal until the output signal get distorted. When this happens slightly reduce the input signal amplitude such that output is maximum undistorted signal. Then measure the magnitude of the input and output waveform. Calculate the Voltage gain. **5. Connect the bootstrap circuit Rb and Cb between the emitter and base as shown in the circuit. Repeat the steps 3 to 5**

To measure Zi and Zo:

Procedure

1. Connect the circuit as shown in figure.
2. Set the DRB to minimum resistance (0Ω), I/P sine wave amplitude to 1V p-p, I/P sine wave frequency to 10 KHz.
3. Measure Vo (p-p). Let Vo=Va
4. Increase DRB till Vo=Va/2.the corresponding DRB value gives Zi.

To measure Zo (Output Impedance):
Procedure:

1. Connect the circuit as shown in figure. Set the DRB to its maximum resistance value, I/P sine wave amplitude to 1V p-p, Frequency to 10 KHz.
2. Measure Vo p-p, let Vo = Vb
3. Decrease DRB till Vo =Vb/2.

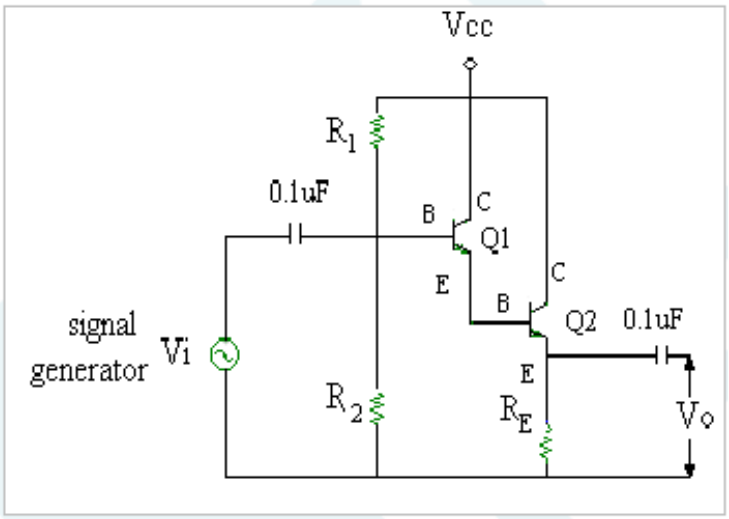
The corresponding DRB value gives Zo.
To find the current gain:

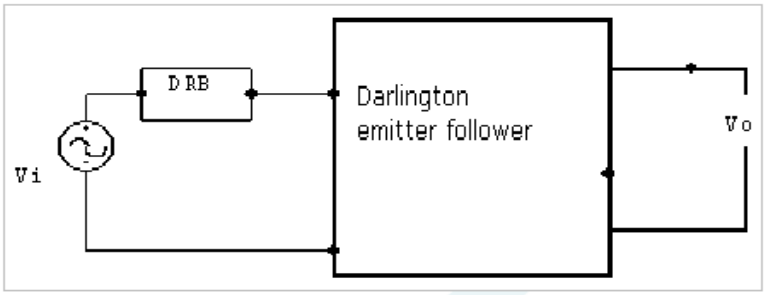
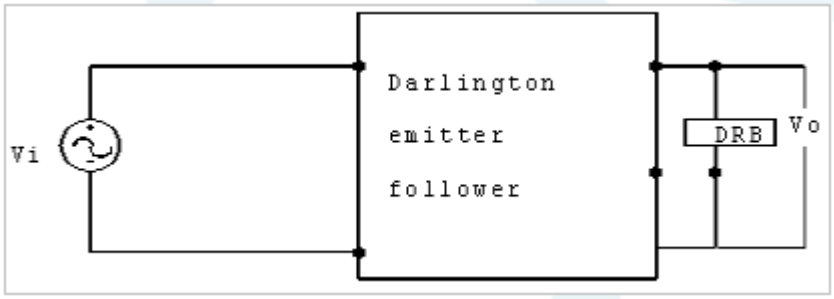
$$Ai = Io/Ii = (Vo/Zo)/(Vi/Zi) = (Vo/Vi) * (Zi/Zo)$$

Current gain Ai ≈ Zi / Zo, since (Vo/Vi) = 1

7 Block, Circuit, Model Diagram, Reaction Equation, Expected Graph

Circuit Diagram:
Darlington emitter follower without bootstrap



		Vi=signal generator 1v(p-p), Vo = measured using CRO, R1 = 1MΩ, R2 = 1.5 MΩ, Re= 2.2kΩ, Vcc = 10V, $C_1 = C_2$ =0.1 μ F (ceramic). **To measure Zi and Zo** To measure Zi (Input Impedance)  **To measure Zo (Output Impedance)** 
8	Observation Table, Look-up Table, Output	Write down the reading and do the calculations for the gain, input & output impendances
9	Sample Calculations	**Darlington emitter follower without bootstrap** **Design of Bias circuit** Let Vce = 5V, Icq=2mA, β= 100 (Q point of transistor Q2) Then Vcc = 2Vce=2 x 5 =10V Ie = Ic = 2 mA V_{Re} = Vcc - Vce= 10 – 5 = 5V Re= V_{Re} / Ie = 5V / (2mA) = **2.2K Ω** (Choose) V_{R2} -Vbe1 - Vbe2 – V_{R3} = 0 and V_{R2} = Vbe1 + Vbe2 + V_{Re} = 0.6 + 0.6 + (Ie.Re) = 1.2 + (5) = 6.2V $V_{CC} = V_{R1} + V_{R2}$ V_{R1}= Vcc – V_{R2} = 10 – 6.2 = 3.8 V Ie1= Ib2 = Ic / hfe = 2 mA / 100 = 0.2mA

		Ib1=Ie1 / hfe = 0.2mA / 100 = 0.02mA R1 = V_{R1}/ (10 (Ib1)) = 3.8 / (10 x 0.02mA) = 1.9 MΩ **Choose R1=1 MΩ** **R2= V_{R2} / (9 Ib) = 7.2 / (9 x 0.02mA) = 3.4 MΩ Choose R2=1.5 MΩ**
10	Graphs, Outputs	
11	Results & Analysis	**Result:** Thus the Darlington's Emitter follower was designed and studied
12	Application Areas	In some Capacitor to power the high-side NMOS driver.
13	Remarks	
14	Faculty Signature with Date	

Parameters	Av =Vo/Vi	Zi	Zo	Ai
Without Bootstrap				
With bootstrap				

Experiment 05 : COMMON EMITTER bjt Amplifier

-	**Experiment No.:**	5	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain-bandwidth product from its frequency response.						
2	Course Outcomes	Design BJT common emitter amplifier & determine the Gain & Frequency response.						
3	Aim	To design a common emitter amplifier under voltage divider bias with and without feedback.						

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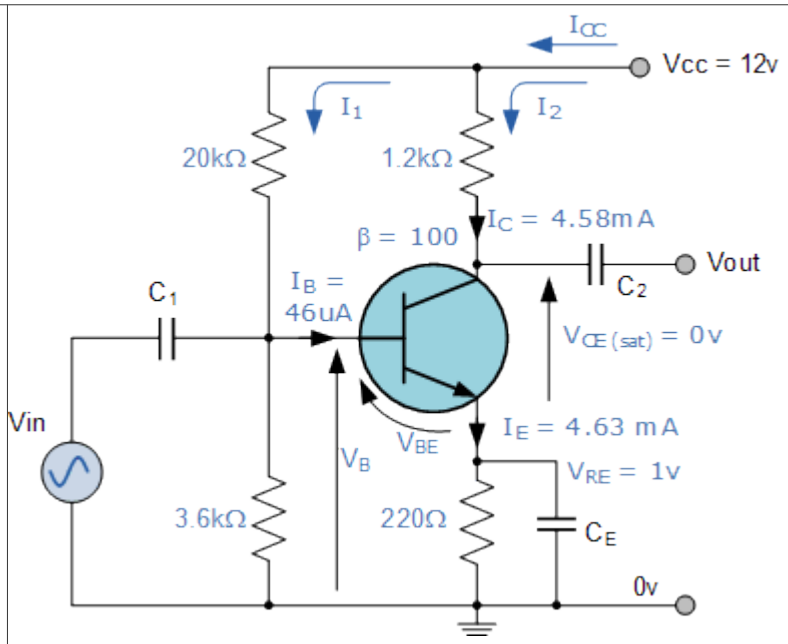
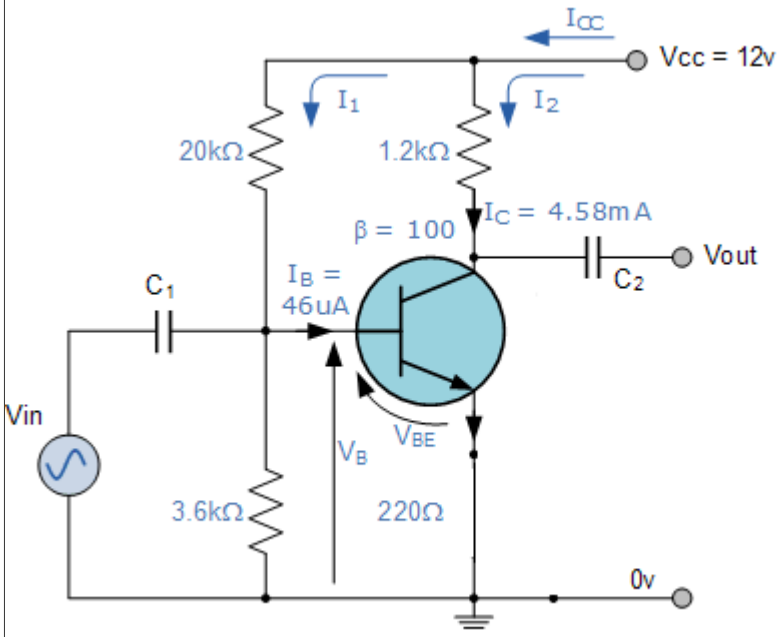
4	Material / Equipment Required	Bread board, NPN transistor, Resistors, Capacitors, VRPS, Signal generator, CRO for testing, Probes, wires, DRB, Multimeter for testing
5	Theory, Formula, Principle, Concept	**Thoery:** The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing". This type of biasing arrangement uses two resistors as a potential divider network across the supply with their center point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits. This method of biasing the transistor greatly reduces the effects of varying Beta, (β) by holding the Base bias at a constant steady voltage level allowing for best stability. The quiescent Base voltage (Vb) is determined by the potential divider network formed by the two resistors, R1, R2 and the power supply voltage Vcc as shown with the current flowing through both resistors.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Procedure:** 1. Connect the circuit as per the circuit diagram. 2. Apply input of 1v p-p. 3. Measure the output voltage at collector. 4. Calculate the gain. 5. Vary the input frequency from 100 Hz to 1MHz and plot the bandwidth of the amplifier.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit Diagram:** **a) without feedback**



B) with feedback



8	Observation Table, Look-up Table, Output	**OBSERVATIONS:**

S.NO	Frequency(Hz)	INPUT VOLTAGE(V_i)	OUTPUT VOLTAGE(V_0)	VOLTAGE GAIN A_v= (V0/V_i)

9 Sample Calculations

Design:

A common emitter amplifier circuit has a load resistance, R_L of 1.2kΩs and a supply voltage of 12v. Calculate the maximum Collector current (Ic) flowing through the load resistor when the transistor is switched fully "ON" (saturation), assume Vce = 0.

$$I_{C(MAX)} = \frac{V_{CC} - V_{RE}}{R_L} = \frac{12 - 1}{1200} = 9.2\text{mA}$$

Generally, the quiescent Q-point of the amplifier is with zero input signal applied to the Base, so the Collector sits about half-way along the load line between zero volts and the supply voltage, (Vcc/2). Therefore, the Collector current at the Q-point of the amplifier will be given as:

$$Ic_{(Q)} = \frac{\frac{12-1}{2}}{1200} = \frac{5.5}{1200} = 4.58\text{mA}$$

If we assume a Beta (β) value for the transistor of say 100

$$\beta = \frac{I_C}{I_B}$$

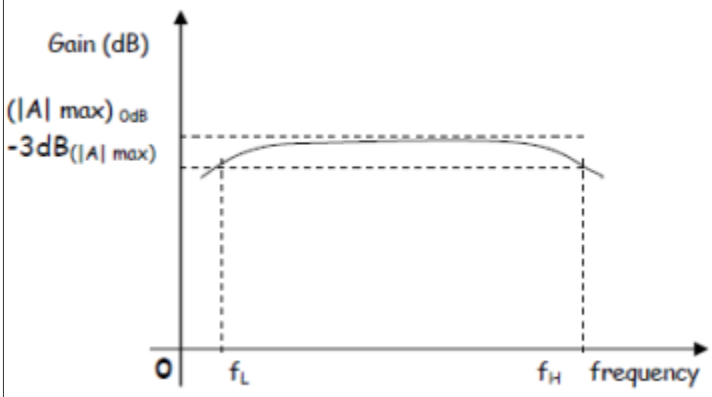
$$\therefore I_B = \frac{I_C}{\beta} = \frac{4.58mA}{100} = 45.8\mu A$$

$$R_1 = \frac{V_{CC} - \left(V_{(RE)} + V_{(BE)}\right)}{11 \times I_B} = \frac{12 - 1.7}{504 \times 10^{-6}} = 20.45k\Omega$$

$$I_E = I_C + I_B = 4.58mA + 45.8\mu A = 4.63mA$$

$$R_E = \frac{V_{RE}}{I_E} = \frac{1v}{4.63mA} = 216\Omega$$

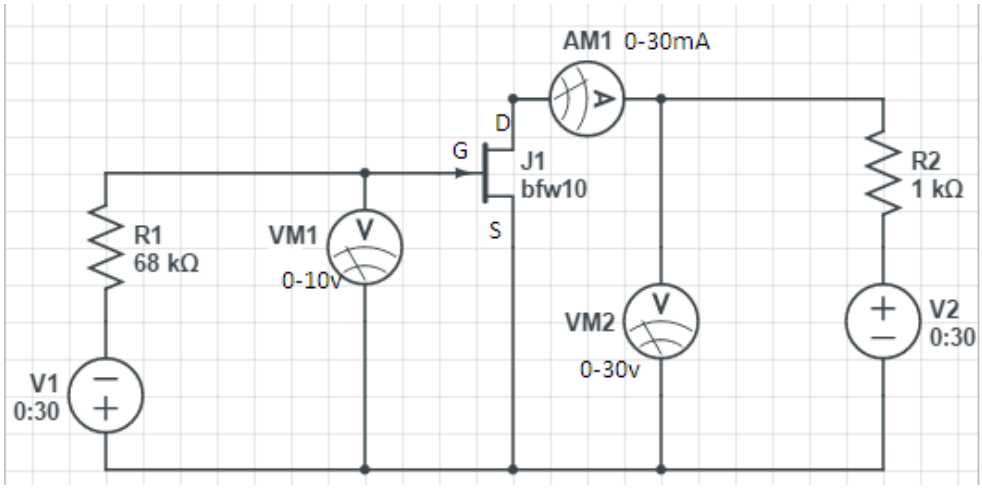
$$R_1 = 20k\Omega,\ R_2 = 3.6k\Omega,\ R_L = 1.2k\Omega,\ R_E = 220\Omega$$

10	Graphs, Outputs	**Nature of Graph:** 
11	Results & Analysis	**Result:** Transistor in CE configuration amplifier under voltage divider bias with feedback is verified with gain=

		And bandwidth = **Result:** Transistor in CE configuration amplifier under voltage divider bias with feedback is verified with gain= And bandwidth =
12	Application Areas	Apply voltage divider bias to find gain bandwidth & frequency response
13	Remarks	
14	Faculty Signature with Date	

Experiment 06: Characteristics of Junction Field Effect Transistor

-	**Experiment No.:**	6	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.						
2	Course Outcomes	Plot the transfer & drain characteristics of JFET & do the resistance & conductance calculations						
3	Aim	To plot the characteristic curve of a given FET and determine r_d,g_m,μ, I_{dss}, V_p						
4	Material / Equipment Required	Lab Manual Regulated Power Supply (0-30V) -2 numbers, Ammeter (0-30 mA)-2 numbers, Voltmeter (0-30V)-2 numbers. FET-(Bfw-10), 68K, 1K resistors.						
5	Theory, Formula, Principle, Concept	**Theory:** FET is a voltage controlled electronic device. It has got 3 terminals. They are Source, Drain and Gate. When its gate is biased –ve with respect to the source, the PN junction are reverse biased and depletion region are formed. The channel is more lightly doped than P type gate. So the depletion region penetrates deeply into the channel. The result is that the channel is narrowed and its resistance is increased and I_d is reduced. When the –ve bias voltage is further increased the depletion region meet at the center and I_d is cutoff completely.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	Drain Characteristics 1. Connect the circuit as per the circuit diagram. 2. Set the gate voltage V_{GS} =0V. 3. Vary the V_{DS} in steps of 1V and note down the corresponding I_d. 4. Repeat the same procedure for V_{GS} =-1V. 5. Plot the graph for V_{DS} Vs I_d for constant V_{GS}.						

		Procedure: Transfer Characteristics 1. Connect the circuit as per the circuit diagram. 2. Set the drain voltage V_{DS} =5V. 3. Vary the V_{GS} in steps of 1V and note down the corresponding I_d. 4. Repeat the same procedure for V_{DS} =10V. 5. Plot the graph for V_{GS} Vs I_d for constant V_{DS}.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit Diagram:** 
8	Observation Table, Look-up Table, Output	Drain Characteristics:

V_{GS}=0v		V_{GS}=-1v	
V_{DS}(v)	I_d(mA)	V_{DS}(v)	I_d(mA)

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Transfer Characteristics:

V_{DS}=5v		V_{DS}=10v	
V_{GS}(v)	I_d(mA)	V_{GS}(v)	I_d(mA)

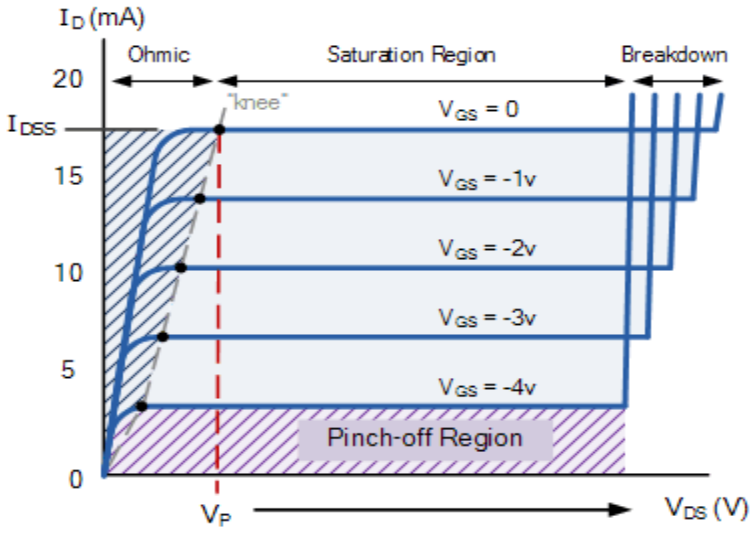
9 Sample Calculations

FET Parameter Calculations:

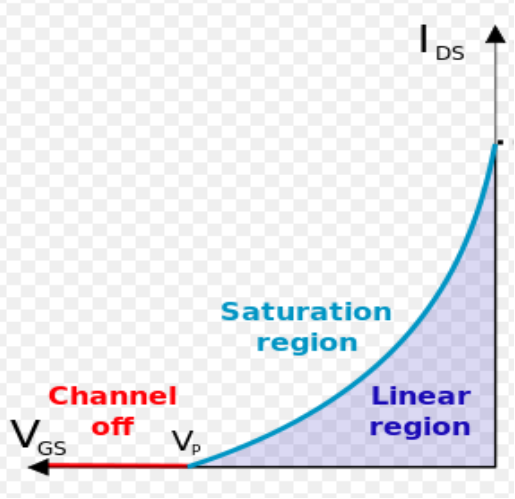
- Drain Resistance $r_{d=} \Delta V_{DS/} \Delta I_d$
- Tran conductance $g_{m=} \Delta I_{d/} \Delta V_{GS}$
- Amplification Factor=μ= r_{d*} g_m

10 Graphs, Outputs

Output Characteristic Graph:



Input Characteristics Graph:

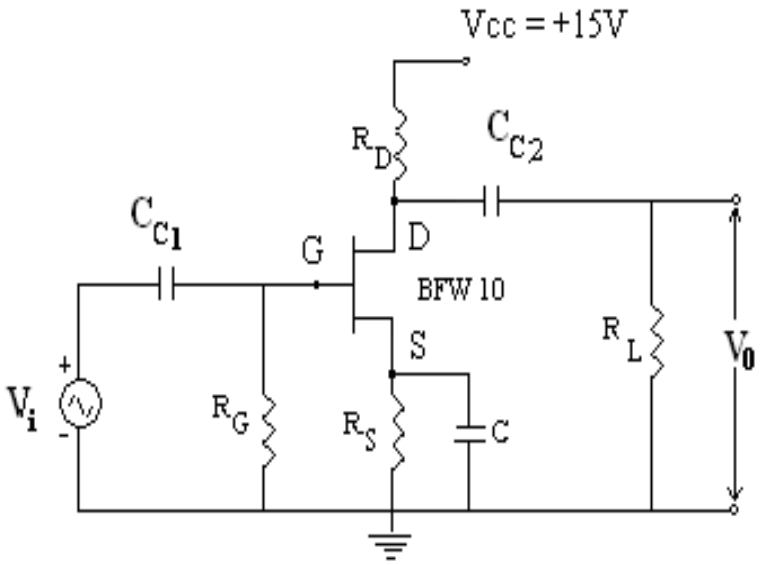
		
11	Results & Analysis	**Result:** Thus the drain and transfer characteristics of given FET is plotted. • Drain Resistance $r_{d=}$ • Tran conductance $g_{m=}$ • Amplification Factor=μ= • $I_{DSS=}$ • Pinch off Voltage =V_p=
12	Application Areas	Used in buffer amplifier,electronic switch, phase shift oscillator etc
13	Remarks	
14	Faculty Signature with Date	

Experiment 07 : Common source JFET/MOSFET

-	**Experiment No.:**	7	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.						
2	Course Outcomes	Construct JFET/MOSFET and Analyze & plot the frequency response graph.						
3	Aim	Design RC Coupled single stage FET amplifier and determine the gain, Frequency response, input and output impedance.						
4	Material /	Lab Manual Bread board, NPN transistor, Resistors, Capacitors, VRPS, Signal generator,						

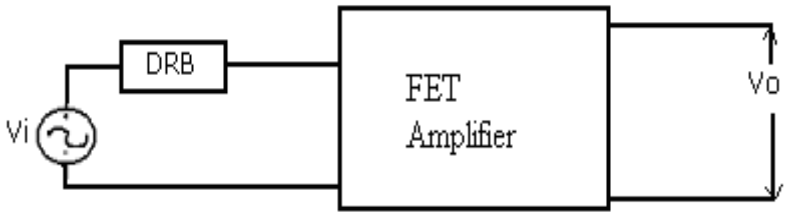
	Equipment Required	CRO for testing, Probes, wires, DRB, Multimeter for testing
5	Theory, Formula, Principle, Concept	**Theory:** with the field effect transistor (FET) , the use of RC coupling can present quite a problem when a load resistance is placed in the drain current. Drain current is set by the bias voltage applied to the gate of the FET and unfortunately the drain current versus gate voltage characteristic of the FET varies from sample to sample of the same transistor type. If a resistance loaded drain is used, gate bias must be set to suit the individual transistor. Resistor Rs is used to provide DC feedback for stabilization of the operating point but this must be by-passed by capacitor Cs to prevent negative feedback at signal frequency. The value of Cs should be selected such that its reactance is not greater than one tenth of the value of Re at the lowest frequency of operation. Capacitor C3 provides DC isolation between the collector circuit and the following load circuit or following stage.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Procedure:** 1. Connect the circuit as shown above. 2. Apply a sine wave signal of amplitude 100 mV from signal generator. 3. Keep the frequency of the signal generator in mid band range i.e., around 2 KHz. Increase amplitude of the input signal till the output signal is undistorted.(CRO at output). 4. Measure Vi amplitude =_____V for corresponding maximum undistorted output. 5. Measure Vo amplitude =_____V 6. The ratio of (Vo/Vi) max gives the maximum undistorted gain of the amplifier. 7. Now vary the input sine wave frequency from 100 Hz to 1 MHz in suitable steps. Measure output voltage amplitude at each step using CRO.(See that amplitude of Vi remains constant throughout the frequency range.) 8. Tabulate the results in the tabular column shown below. 9. Plot the frequency response i.e., frequency versus Gain in dB, determine Bandwidth and G.B.W product.

		To measure Zi: **Procedure**: 1. Connect the circuit as shown in above figure 2. Set the following • DRB to 0Ω • Input sine wave amplitude to say 50 mV • Input sine wave frequency to any mid frequency say 10 KHz. 3. Measure amplitude of Vop-p. Let Vo=Va say 4. Increase DRB (keeping Vi constant) till Vo=Va/2.The corresponding DRB gives the input impedance Zi in RC coupled amplifier **To measure Zo:** **Procedure**: 1. Connect the circuit as shown in the above figure 2. Set the following • DRB to its maximum resistance value. • Input sine wave amplitude to about 50 mV • Input sine wave frequency to 10 KHz. 3. Measure Vop-p. Let Vo=Vb 4. Decrease DRB from its maximum value till Vo=Vb/2.The corresponding DRB gives the output impedance Zo.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit diagram:**

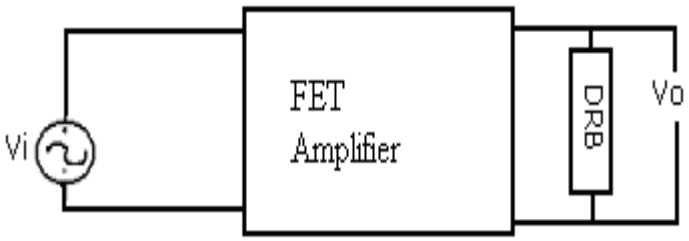


Vi=signal generator 100mv(p-p), Vo = measured using CRO, R_G=2.2MΩ, R_D=2.7KΩ, Rs=1KΩ,
R_L=10KΩ, Cs=47μF (electrolytic), Cc_1= Cc_2 = 0.1 μ F (ceramic).

To measure Zi

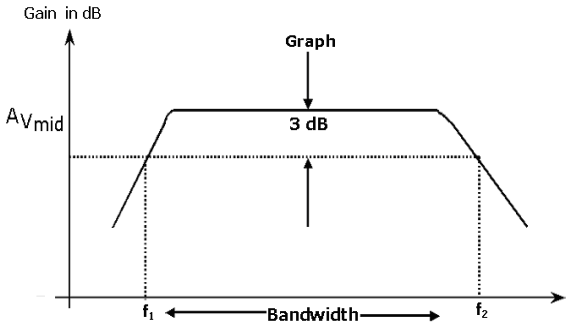


To measure Zo:



8	Observation Table, Look-up Table, Output	**Tabular column:** **Take the readings for 100 Hz to 1MHz in 100kHz steps, Note down Vi (P-P)……**

Frequency (Hz)	Output Voltage (P-P) (Volts)	Voltage Gain Av = V_o / V_i	Gain in dB =20 log (V_o / V_i)

9	Sample Calculations	**Design:** Assume the gain of the FET amplifier to be equal to 10 From specifications of FET BFW 10, Let I_D = 2mA , I_{DSS} = 10mA, V_P = -3V V_{GS} = -2V Let V_{DD}= 10V then V_{DS}= 10/2 = 5V $I_D = I_{DSS}[1-V_{GS}/V_P]^2$ Simplifying we get V_{GS}=1.67V We know Vs = I_D × Rs Assuming I_D = Is=2mA Vs = Is × Rs Therefore Rs = Vs / Is = $-V_{GS}$ / Is = 1.67 / 2mA = 820Ω To find R_D, $V_{DD} = V_{DS}+I_D*R_D+Vs$ $R_D = [V_{DD} - V_{DS} - Vs]/ I_D$ = **[10-5-1.67]/2mA= 1.6 Kohm.** **Choose R_D=1.5KΩ** The input resistance of FET is very high hence R_G=2MΩ **Choose R_G=2.2MΩ** Bypass capacitor **C_S=0.22µF** **Coupling capacitors $C_{C1} = C_{C2}$ = 0.1µF**
10	Graphs, Outputs	**Frequency response:** 

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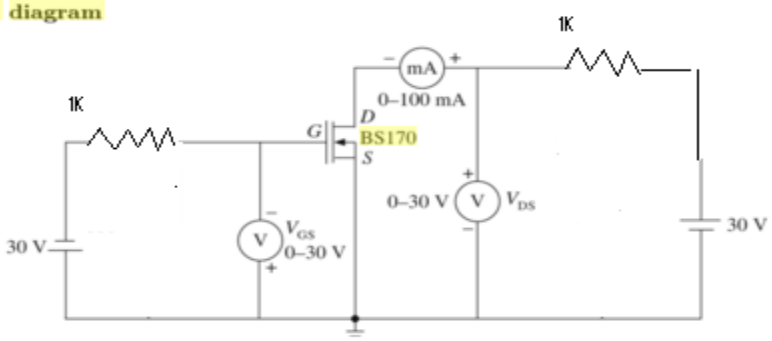
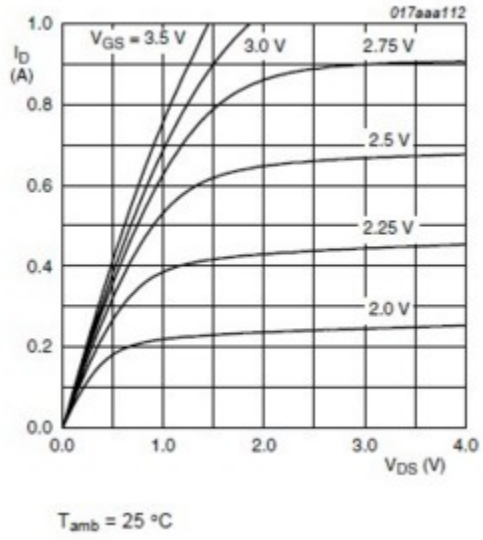
		f_1: Lower Cut-Off Frequency f_2: Higher Cut-Off Frequency A_V:Voltage Gain = $20\log_{10}(V_0/V_i)$ A_{Vmid}: Voltage Gain at mid-band f_2-f_1:Band width of the amplifier **3dB = $20\log_{10}(0.707)$**
11	Results & Analysis	**Result:-** Thus the single stage FET Amplifier was designed and studied. Gain = Bandwidth = Gain-Bandwidth product = Input Impedance = Output Impedance =
12	Application Areas	widely used for switching and amplifying electronic signals in the electronic devices.
13	Remarks	
14	Faculty Signature with Date	

Experiment 08 : n-channel MOSFET

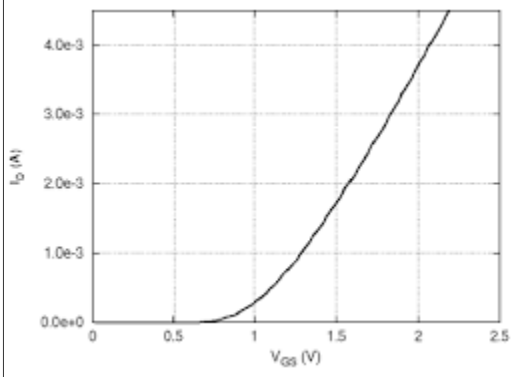
-	**Experiment No.:**	8	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.						
2	Course Outcomes	Calculate & Plot the transfer & drain characteristics of N-channel MOSFET						
3	Aim	Design N-channel MOSFET and determine the drain resistance, mutual conductance and amplification factor.						
4	Material / Equipment Required	Lab Manual MOSFET, Power supply, Voltmeters, Ammeters, Resistances						

5	Theory, Formula, Principle, Concept	**Theory:** The **metal–oxide–semiconductor field-effect transistor** (**MOSFET**, **MOS-FET**, or **MOS FET**) is a type of transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals,[1] the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. The main advantage of a MOSFET over a regular transistor is that it requires very little current to turn on (less than 1mA), while delivering a much higher current to a load (10 to 50A or more). In *enhancement mode* MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts *via* the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the *inversion layer*. The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate (see article on semiconductor devices). In the less common *depletion mode* MOSFET, detailed later on, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and conductivity is decreased by application of a field that depletes carriers from this surface layer.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	Step 1: start by Designing the circuit using bread board Step 2: Note down the readings Step 3: do the calculations for drain resistance, mutual conductance and amplification factor. Step 4: Disconnect the circuit

7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit diagram** 
8	Observation Table, Look-up Table, Output	**Observation:** Drain Characteristics V_{GS}=0v | V_{GS}=-1v V_{DS}(v) | I_d(mA) | V_{DS}(v) | I_d(mA) Transfer Characteristics V_{DS}=5v | V_{DS}=10v V_{GS}(v) | I_d(mA) | V_{GS}(v) | I_d(mA)
9	Sample Calculations	
10	Graphs, Outputs	**Graph:** **Output Characteristics:**



Input Characteristics:



11	Results & Analysis	**Result:** Thus the drain and transfer characteristics of given FET is plotted. • Drain Resistance $r_{d=}$ • Tran conductance $g_{m=}$ • Amplification Factor=μ=
12	Application Areas	Switching circuits
13	Remarks	
14	Faculty Signature with Date	

Experiment 09 : class B push pull power amplifier

-	**Experiment No.:**	9	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.						
2	Course Outcomes	Understand the Working of class B push pull power amplifier						
3	Aim	Design class B push pull power amplifier and determine the efficiency.						
4	Material / Equipment Required	Lab Manual						
5	Theory, Formula, Principle, Concept	To see the working of class B push pull power amplifier To do the calculations for efficiency						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	Step 1: start by Designing the circuit using bread board Step 2: see the working & Note down the readings Step 3: do the calculations for efficiency Step 4: Disconnect the circuit						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output	Write down the reading and do the calculations for efficiency						
9	Sample Calculations							
10	Graphs, Outputs							
11	Results & Analysis							
12	Application Areas	used in low-cost design devices and mobile devices						
13	Remarks							
14	Faculty Signature with Date							

Experiment 10 : RC-Phase shift Oscillator using FET

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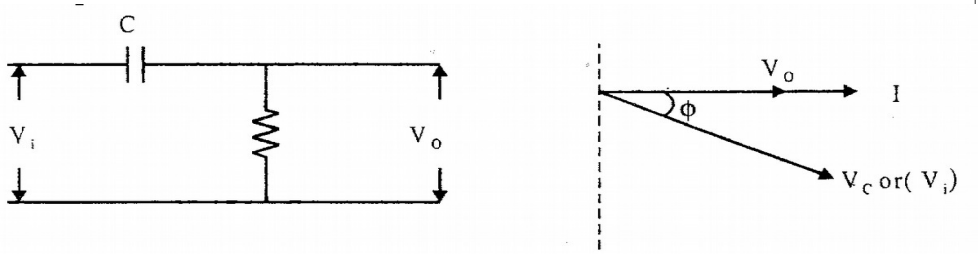
-	**Experiment No.:**	10	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.						
2	Course Outcomes	Construct & test the RC-phase shift oscillator using FET						
3	Aim	Writing and testing for the performance of BJT-RC Phase shift Oscillator for f_0 <10k H_z (To design and verify the performance of RC phase shift Oscillator)						
4	Material / Equipment Required	Lab Manual Power supply (0-30V), Resistors, Capacitors, Potentiometer, transistor (SL100).						
5	Theory, Formula, Principle, Concept	**Theory:** RC phase shift Oscillator basically consists of an amplifier and feed back network consisting of resistors and capacitors in ladder fashion. The basic RC circuit is as shown below  The current I is in phase with Vo, whereas the capacitor voltage Vc lags the current I by φ (90^0→Ideal value). OR the output voltage Vo leads the I/P voltage Vi by angle φ is adjusted in practice, equal to 60^0. RC network is used in feedback path. In Oscillator, feedback network must introduce a phase shift of 180^0 to obtain total phase shift around a loop as 360^0.Thus three Rc network each provide 60^0 phase shift is cascaded, so that it produces total 180^0 phase shift. The Oscillator circuit consisting amplifier and Rc feedback network is as shown below.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Make the circuit connections as shown in Fig.1, the output Vo is obtained on CRO 2. The 10 KΩ pot is adjusted to get a stable output on the CRO. 3. The frequency of Oscillations is measured using CRO and then compared with the theoretical values. 4. With respect to output at point P, the waveforms at point Q, R and S are observed on the CRO. We can see the see the phase shift at each point being 60^0, 120^0 and 180^0 respectively.						

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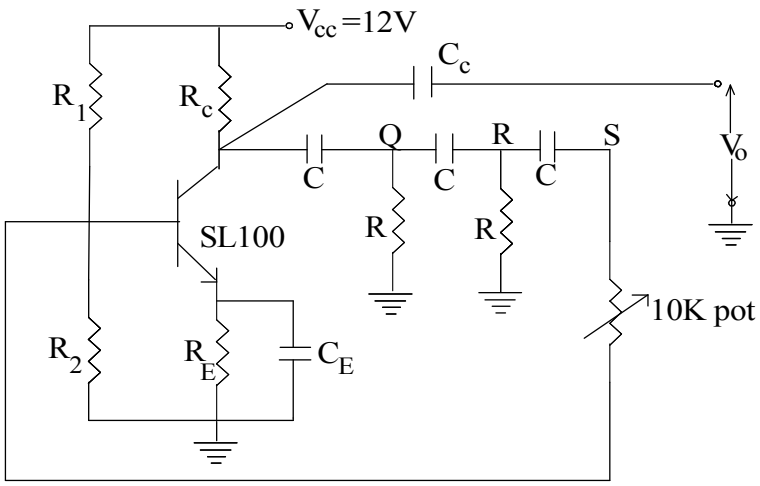
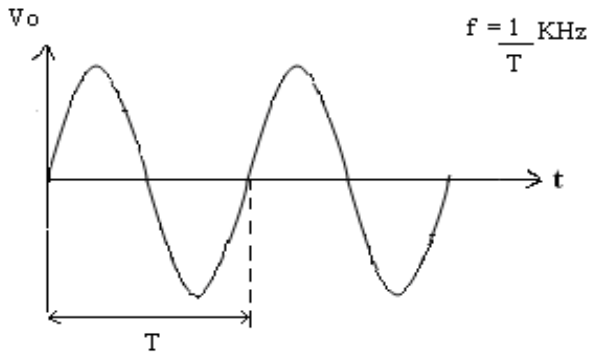
		NOTE: The value of all three capacitors C is changed and the frequency of Oscillation can be changed to new value and is measured again.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit Diagram:**  Vo = measured using CRO, R_1=22KΩ, R_2=4.7KΩ, Rc=1KΩ, Re=470Ω, Ce=47μF (electrolytic), $Cc_1 = Cc_2$ =0.1 μ F (ceramic).R =3.9 K, C = 0.01uF
8	Observation Table, Look-up Table, Output	Write down the reading & wave forms and do the calculations for frequency of output waveform.
9	Sample Calculations	**Design:** *Let Vcc=10V, Ic=2mA, β=50* V_{CE}=10/2 = 5V V_E=1/10th Vcc=10/10=1V $R_E=V_E/I_E$ = 1/2mA=500Ω **Choose R_E=470Ω** Using KVL loop $Vcc=I_CR_c+V_{CE}+V_E$ R_C = (10-5-1)/2mA = 2 KΩ **Choose R_C=2.2kΩ** From biasing circuit $VB=V_{BE}+V_E$=0.7+1=1.7V $I_C=\beta I_B$ I_B=0.04mA Assume $10I_B$ flowing in R_1 and $9I_B$ flowing in R_2

		$R_1=(Vcc-V_B)/10I_B=22.4k\Omega$ **Choose $R_1=22k\Omega$** $R_2=V_B/9I_B=4.69K\Omega$ **Choose $R_2=4.7k\Omega$** Bi-pass capacitor is selected by taking lower cut off frequency f1=300Hz hie=1.2KΩ $X_{CE}=1/2\pi fC_E = Re/10$ **$C_E=47\mu F$** **$C_{C1} = C_{C2} = 0.1\mu F$** **Design of phase shifting network** The frequency of oscillations is determined by phase shifting network. The oscillating frequency for the above circuit is given by $f = 1/2\Pi RC$ Let f = 2KHz and R = 2.2KΩ caluc\C = 0.01μF
10	Graphs, Outputs	**Specimen graph:** 
11	Results & Analysis	**Result:** Designed frequency = --------- Actual frequency = ---- Phase shift between P & Q --- P & R ----

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		P & S ---
12	Application Areas	musical instruments, voice synthesis and in GPS units since they work at all audio frequencies.
13	Remarks	
14	Faculty Signature with Date	

Experiment 11 : Hartley Oscillator & Colpitts Oscillator

-	**Experiment No.:**	11	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a) Hartley Oscillator (b) Colpitts Oscillator						
2	Course Outcomes	Determine the frequency response of Hartley & Colpitts oscillator						
3	Aim	To understand the design aspects and feature of the Hartley and Colpitts oscillator using BJT.						
4	Material / Equipment Required	Lab Manual Bread board, NPN transistor SL100, Resistors, Capacitors, VRPS (0-30Vdc), Decade Capacitor Box, CRO for testing						
5	Theory, Formula, Principle, Concept	**Theory:-** In phase shift oscillator, RC circuit is used to get the oscillation whose frequency is in the audio range. To get higher frequency of oscillation, feedback circuit to have inductor and capacitors. The oscillators that employ L&C elements are called tuned oscillators. Hartley and Colpitts oscillators belong to LC tuned oscillator. A Hartley oscillator as shown in fig 2 has an Potential divider biased BJT amplifier and LC feedback circuit. Its feedback or tank circuit consists of 2 inductor in series and one capacitor in parallel. Colpitts oscillator is similar to the Hartley oscillator except the change in the tank circuit. Here the tank circuit consists of 2 capacitors in series and one capacitor as shown in fig 1. The amplifier is single stage amplifier and has 180^0 phase shift. So this tank circuit provides 180^0 phase shift due to inductor & capacitor connection to make total phase shift of the circuit as 360^0 at the frequency of oscillation. When the feedback is adjusted so that $A\beta = 1$, sustained oscillation occurs at the output.						

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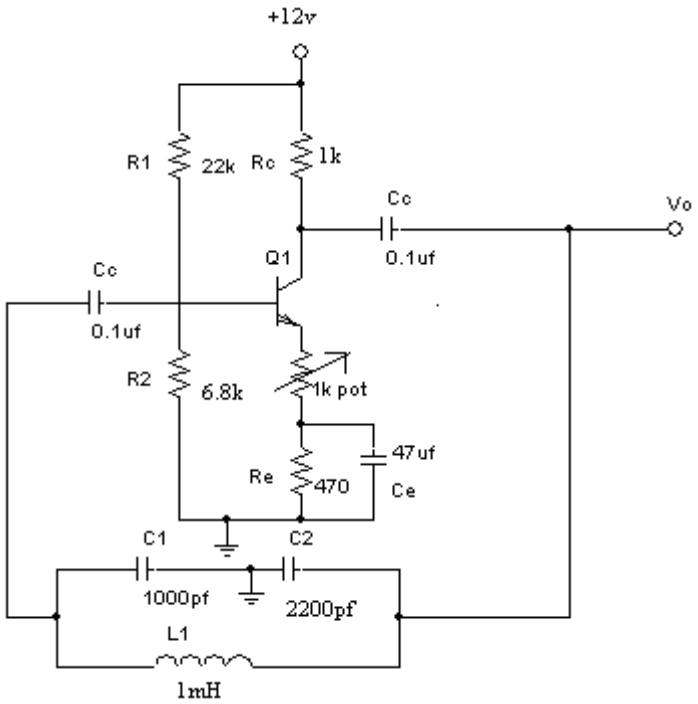
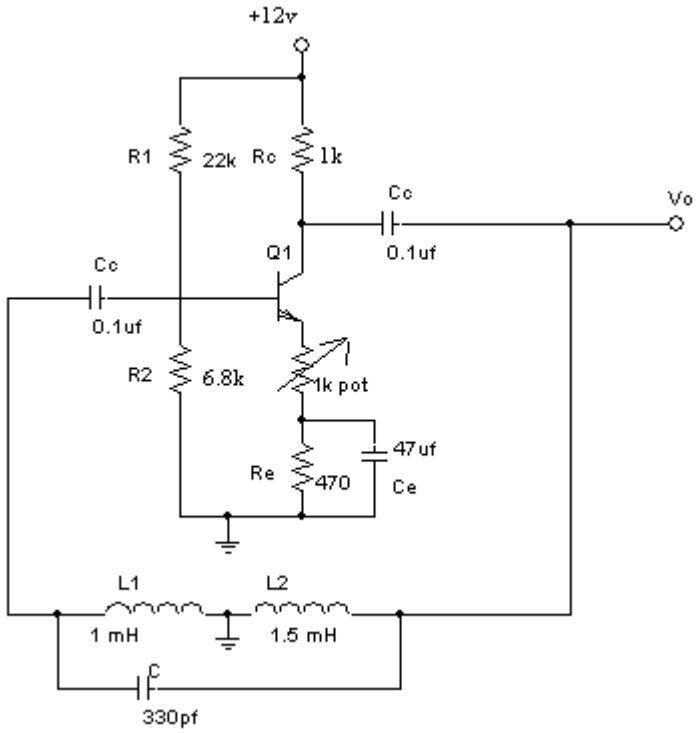
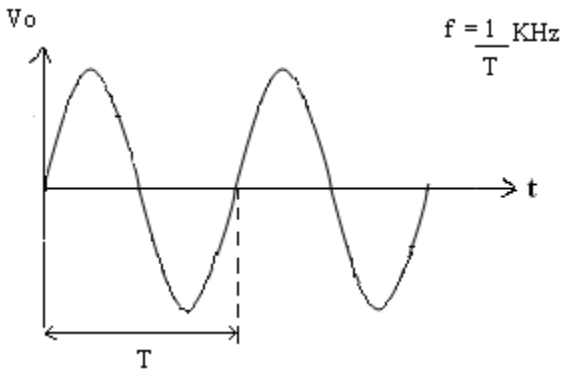
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Design & Draw the circuit, Calculate the component values 2.Connect the components on the bread board as per diagram shown in fig1. 3.Switch on Vcc and verify the biasing circuit and note down the values 4.Also observe the wave form across the output using CRO 5.If wave is not observed, connect a variable 10K or 1K pot in series with Re resistor. Adjust this potentiometer to get the output 6.Draw the waveform on the graph sheet and note down the frequency. 7.Compare this frequency with the expected frequency and find the % error. 8.Repeat this for the Hartley oscillator as shown in figure2
27	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit diagram:** **Colpitts Oscillator**  Vo = measured using CRO, R_1=22KΩ, R_2=6.8KΩ, Rc=1KΩ, Re=470Ω, Ce=47μF (electrolytic), Cc = Cc =0.1 μ F (ceramic).

		Hartley Oscillator:  Vo = measured using CRO, R_1=22KΩ, R_2=6.8 KΩ, Rc=1KΩ, Re=470Ω, Ce=47μF (electrolytic), Cc = Cc =0.1 μ F (ceramic).
8	Observation Table, Look-up Table, Output	Write down the reading and do the calculations for the frequency of oscillation.
9	Sample Calculations	**Design of amplifier:** *Let Vcc=10V, Ic=2mA, β=50* Let V_E=1V V_{CE}=10/2 = 5V $R_E=V_E/I_E$ = 1/2mA=500Ω **Choose R_E=470Ω** Using KVL loop $Vcc=I_CR_c+V_{CE}+V_E$ R_C = (10-5-1)/2mA = 2KΩ **Choose R_C=2.2kΩ** From biasing circuit $VB=V_{BE}+V_E$=0.7+1=1.7V

		$I_C=\beta I_B$, $I_B=0.04mA$ Assume $10I_B$ flowing in R_1 and $9I_B$ flowing in R_2 $R_1=(Vcc-V_B)/10I_B=22.4k\Omega$ **Choose $R_1=22k\Omega$** $R_2=V_B/9I_B=$ **Choose $R_2=4.7k\Omega$** Use **$C_E=47\mu F$** **$C_{C1} = C_{C2} = 0.1\mu F$** **Design of tank circuit for Colpitts oscillator** To design a colpitts oscillator to oscillate at a frequency of 200kHz $f = 1/2\pi\sqrt{LC_{eq}}$ Where C_{eq}= C1C2/(C1+C2) Let **L = 1mH** and f = 200kHz For sustained oscillations, the gain of the amplifier must be ≥ C_1/C_2 i.e, 2.2 Use **C1 = 1000pF; C2 =2200pF** **Design of tank circuit for Hartley oscillator** To design a Hartley oscillator to oscillate at a frequency of 100kHz $f = 1/2\pi\sqrt{L_{eq}C}$ Where $L_{eq} = L_1+L_2$ Let f= 100kHz and C = 330 pF $L_{eq} = 1/[(2\pi f)^2 \times C] = 1/[(2\times3.14\times100)^2 \times 330\ pF]$ L_{eq} =2.5mH Use **L_1 = 1mH ; L_2 = 1.5mH**
10	Graphs, Outputs	**Specimen graph:**

		
11	Results & Analysis	**Result:-** The frequency of oscillation obtained for Hartley Oscillator is equal to ----------kHz The frequency of oscillation obtained for Colpitts Oscillator is equal to ----------kHz
12	Application Areas	Used in radio receivers, oscillations in RF, sensors, mobile and radio communications.
13	Remarks	
14	Faculty Signature with Date	

Experiment 12 : Crystal oscillator

-	**Experiment No.:**	12	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Design and set-up the crystal oscillator and determine the frequency of oscillation.						
2	Course Outcomes	Determine the frequency of oscillation of crystal oscillator						
3	Aim	Design and testing for the performance of BJT- crystal oscillator for f_o > 100KHz						

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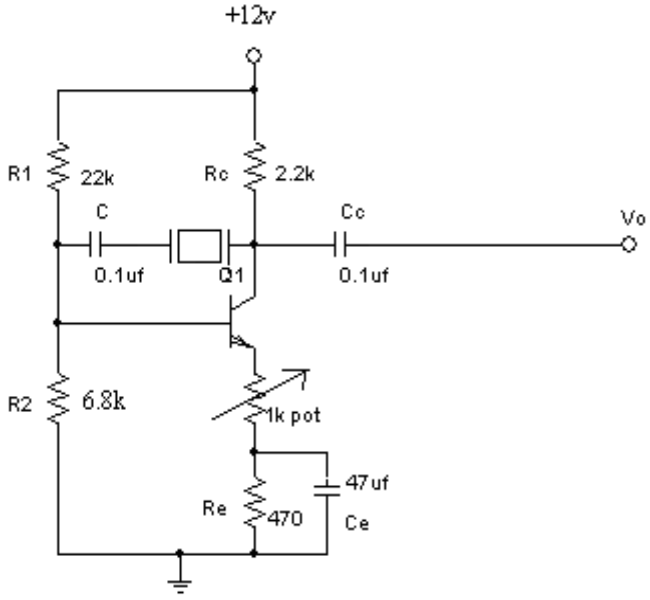
4	Material / Equipment Required	Lab Manual Bread board, transistor SL100, Resistors / Potentiometer, Capacitors, VRPS(0-30V dc), CRO & Multimeter, Probes
5	Theory, Formula, Principle, Concept	**Theory:** A Crystal oscillator is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wrist watches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. Crystal oscillators are made from quartz. A crystal can be operated in the series resonant or parallel resonant mode. In the series mode crystal offers minimum impedance at resonance and in parallel mode it offers maximum impedance and is inductive. Since the parallel resonant frequency of a crystal is slightly higher than its series resonant frequency, the method of connection is important.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**Procedure:** 1. Rig up the circuit as shown in figure. 2. Set VCC to 12v, and check the DC conditions of the amplifier circuit 3. If DC conditions are satisfied, connect the feedback circuit and observe the output at the collector terminal. 4. Adjust the pot connected in series with Re such that output is an undistorted sine wave. Measure the frequency and compare with the crystal frequency value.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit Diagram:** 
8	Observation Table, Look-up Table, Output	Write down the reading and do the calculations for frequency of oscillation.

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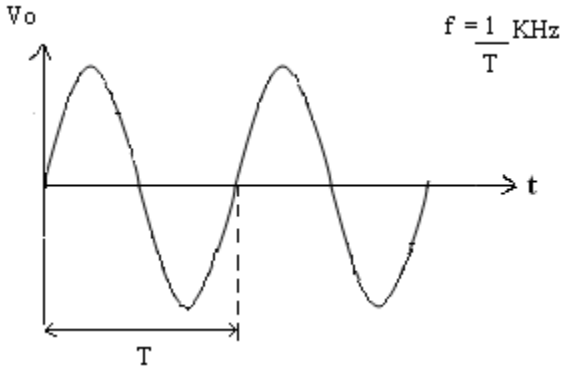
9	Sample Calculations	**Design:** *Let Vcc=10V, Ic=2mA, β=50* Let V_E=1/10 of Vcc = 1/10 = 1V V_{CE} =10/2 = 5V $R_E=V_E/I_E$ = 1/2mA=500Ω **Choose R_E=470Ω** Using KVL loop $Vcc=I_CR_c+V_{CE}+V_E$ R_C = (10-5-1)/2mA = 2KΩ **Choose R_C=2.2kΩ** From biasing circuit $VB=V_{BE}+V_E=0.7+1=1.7V$ $I_C=\beta I_B$ I_B=0.04mA = 40μA Assume $10I_B$ flowing in R_1 and $9I_B$ flowing in R_2 $R_1=(Vcc-V_B)/10I_B$=22.4kΩ **Choose R_1=22kΩ** $R_2=V_B/9I_B$=5k **Choose R_2=4.7kΩ** Use **C_E=47μF, C_C = C = 0.1μF**
10	Graphs, Outputs	**Specimen graph:** 
11	Results & Analysis	**Result:-** Crystal indicated frequency oscillations = ----------MHz.

		The frequency of the output waveform is =----------MHz.
12	Application Areas	frequency-determining component, a wafer of quartz crystal or ceramic with electrodes connected to it.
13	Remarks	
14	Faculty Signature with Date	